REMARKS

Applicants respectfully request entry of this Preliminary Amendment prior to the first Official Action and prior to calculating the fees for the application.

The present application is a reissue of U.S. Patent Application Serial No. 09/347,683.

Status of Claims:

All original claims 1-16 in the original patent are currently pending. Additionally, with this Preliminary Amendment, new claims 17-30 are added and pending as well.

Explanation of Support for Added Claims 17-30:

Support for new independent claim 17 is provided largely by Figure 1 and the disclosure related thereto. Specifically, Figure 1 provides a clock source entering first and second clock frequencies (126 and 128) and a separation sensing circuit (111) that generates an evaluation output (113) as a function of the first frequency separation. A controller (102) receives the evaluation output and provides feedback to the control input (109).

New dependent claim 18 is supported by Figure 6 showing polarity detector (168) coupled to sample clock line (128).

New dependent claim 19 is supported by Figure 6 showing further evaluation output (170) coupled to microprocessor (176).

New dependent claims 20 and 21 are supported by Figure 8 showing a polarity detector (266) embodied on a 7474 clocked D-flip flop.

New dependent claim 22 is supported by Figure 1 where the clock source further includes a voltage controlled oscillator (104) coupled to the control input.

New dependent claims 23 and 24 are supported by Figure 8 which shows a separation sensing circuit (258) embodied on a clocked 7474 D-flip flop. New dependent claim 25 is supported by Figure 5

which illustrates a divider circuit dividing the first and second clock frequencies and generating the transmit and sample frequencies.

New independent claim 26 is supported by the description with respect to Figures 1 and 6 for the same reasons as set forth above with respect to new independent claim 17 and new dependent claim 18.

New independent claim 27 differs primarily from new independent claim 17 in that it indicates that an unstabalized clock is used to generate a first clock frequency. Support for this limitation is found in Figure 1 and the description related thereto which indicates that system clock (106) and the VCO (104) are continuously drifting in time. See column 2, lines 31 and 32.

New dependent claim 28 is supported by Figure 1 and the description related thereto. Claim 28 indicates that the separation output is operably coupled to the control input through the controller.

New claim 29 is supported at least by Figure 6 which shows a polarity sensing circuit 68 coupled to the sample clock and the controller.

New claim 30 is supported at least by the description related to in Figure 1 which indicates that controller (102) further has a correction circuit (117), preferably implemented in software, that corrects the level output as a function of the first frequency separation. See column 2, lines 22-25.

With this preliminary amendment, new claims 17-30, which are broader than the issued claims 1-16, are added. As set forth in detail above, support for each and every of the added claims is provided in the original specification. No new matter has been added. Applicant respectfully requests consideration and allowance of all pending claims 1-30.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to deposit account No. 23-1123.

Respectfully submitted,

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